
Preface

About SPARC International, Inc.

SPARC International, Inc., a not-for-profit consortium for providers of SPARC® products and services, directs the evolution and standardization of the SPARC microprocessor architecture and systems operating environment. Through its committee structure, SPARC International documents this evolution through two primary vehicles: *The SPARC Architecture Manual* and the *SPARC Compliance Definition (SCD)*. These two documents tell vendors of chips, systems, applications, and add-in/add-on hardware how to comply with SPARC International standards, and how to ensure binary level compatibility with all other SPARC products.

To give buyers of SPARC products that same assurance, SPARC International provides compliance testing services to members and grants vendors of SPARC Compliant™ products the right to use the SPARC Compliant trademark. The SPARC Compliant trademark lets buyers know their products have been independently tested for compliance. SPARC International calls the SPARC Compliant trademark the mark of user confidence.

The SPARC Architecture Committee

The SPARC Architecture Manual: Version 8 is a product of the SPARC International Architecture Committee, which at this printing included representatives from Amdahl Corporation, Fujitsu Limited, ICL, LSI Logic, Matsushita, Philips International, Ross Technology, Sun Microsystems, and Texas Instruments.

This committee is open to executive members of SPARC International. Every executive member is investing heavily in the SPARC architecture and applying its best architectural talent to include the features most demanded by customers, and to ensure that every SPARC architecture implementation maintains binary compatibility at the application level.

SPARC Open Licensing

As a result of the Sun Microsystems vision of a truly open standard computing environment, the SPARC architecture has reached a level of openness heretofore unimagined in the computer industry. Not only are a wide range of compatible SPARC chip implementations available from a variety of merchant SPARC licensees, but today anyone can obtain a license to the SPARC architecture for a small fee. To receive an information package, simply sign and return the reply card at the back of this manual to SPARC International. You will receive detailed information, including a license to sign and return with a payment of \$99.00 (U.S. dollars).

This open licensing policy is further evidence of the SPARC standard's radical departure from current business practices. Until the advent of the SPARC standard, large microprocessor concerns maintained exclusive ownership of their standard architectures, and as a result, wielded substantial control over entire technology bases and markets developed around their products.

Today, semiconductor customers all the way through to end-users will realize the benefit of greatly accelerated innovation created by the open SPARC microprocessor standard. As a rapidly-broadening base of engineers implement the SPARC architecture, the base of compatible and complementary SPARC microprocessor products will expand as well to the advantage of both vendors and users.

Note: Rights to specific SPARC microprocessor implementations are the property of their respective developers.

Version 8 Specification

This book specifies Version 8 of SPARC, the **S**calable **P**rocessor **A**rchitecture. It supersedes the Version 7 SPARC document, which has evolved for over three years. Since the publication of Version 7, several commercial sources have released SPARC processors. All of them conform to the Version 7 architecture.

Upward Compatibility

SPARC Version 8 is upward-compatible from Version 7; all Version 7 conformant software will run on Version 8 conformant processors with one minor exception discussed in a following section. The Version 8 changes are enhancements to the architecture; the most obvious is the addition of Integer Multiply and Divide instructions. For a detailed list of changes, refer to the *What's New? – Architecture* section that follows.

Audience for this Manual

Audiences for this specification include implementors of the architecture and developers of SPARC system software (simulators, compilers, debuggers, and operating systems, for example). Software developers who need to write SPARC software in assembly language will also find this information useful.

Where to Start?

If you are new to the SPARC architecture, read Chapters 1 and 2 for an overview. Then look into the following chapters and appendixes for more details on your areas of interest.

If you are already familiar with Version 7, you will want to review the list of changes at the end of the Preface. For additional detail, review Appendix B for each of the new or changed instructions, read Chapter 6 (*Memory Model*), Chapter 7 (*Traps*), and Appendixes J (*Programming with the Memory Model*) and K (*Formal Specification of the Memory Model*).

Manual Contents

The first chapter describes the background, design philosophy, and high-level features of SPARC, and reviews the typographic conventions used in the manual. Chapter 2 is an overview of the SPARC architecture: its organization, instruction set, and trap model. Subsequent chapters describe the SPARC data types, registers, instructions, memory model, and traps in detail.

Appendixes follow the chapters and include the following:

- Appendix A, *Suggested Assembly Language Syntax*, defines syntactic conventions used in the appendixes for the suggested SPARC assembly language. It also lists “synthetic instructions” that may be supported by SPARC assemblers for the convenience of assembly language programmers.
- Appendix B, *Instruction Descriptions*, contains definitions and all instructions for the SPARC assemblers for the convenience of assembly language programmers, including tables showing the recommended assembly language syntax for each instruction.
- Appendix C, *ISP Descriptions*, defines the architecture using a formal algorithmic (Instruction Set Processor, or ISP) notation.
- Appendixes D, E, and G, respectively, contain general SPARC software considerations, SPARC ABI software considerations, and example multiplication/division algorithms.
- Appendix F contains tables detailing all opcodes and condition codes.
- Appendixes G through N contain the Reference MMU architecture, programming with the SPARC memory model, a formal description of the SPARC memory model, and characterizations of existing SPARC implementations.

What’s New? — Architecture

Changes to the SPARC architecture since Version 7 are in four main areas: the memory model, trap model, data formats, and instruction set.

Enhanced Memory Model

Version 8’s memory model is an upward-compatible extension of the Strong Consistency model implicitly assumed in Version 7. The new model allows building of higher-performance memory systems in either uniprocessor or shared-memory multiprocessor SPARC applications.

Enhanced Trap Model

Trap categories have been renamed since Version 7; the correspondence is as follows:

<u>SPARC Version 7</u>	<u>SPARC Version 8</u>
Synchronous Trap	→ Precise Trap
Asynchronous Trap	→ Interrupting Trap
Floating-Point/Coprocessor Trap	→ Deferred Trap

The Version 8 trap model enhancements give SPARC implementors more latitude in their designs. The privileged and essentially user-code-transparent trap architecture includes some new trap types. It also allows for new, implementation-specific traps.

A given trap may be implemented as either “precise” or “deferred”, although each implementation must provide a way to handle traps precisely. Chapter 7 describes the enhanced trap model in detail.

Data Formats

Quad (128-bit) precision data format replaces the Extended (96-bit)-precision format. No existing SPARC application code uses Extended-precision floating-point arithmetic. So, although this one change is not strictly upward-compatible with SPARC Version 7, the impact is insignificant.

Instruction Set

Version 8 modifies the definitions of some SPARC instructions as follows:

- Extended-precision floating-point operations are now Quad-precision operations
- IFLUSH has been renamed FLUSH; its definition has expanded to encompass multiprocessor systems and processor implementations with separate instruction and data memories.

A few instructions have been added to the Version 8 architecture:

- Store Barrier instruction (STBAR)
- Integer Multiply instructions (SMUL, SMULcc, UMUL, UMULcc)
- Integer Divide instructions (SDIV, SDIVcc, UDIV, UDIVcc)
- Floating-point Multiply Single to Double (FsMULd)
- Floating-point Multiply Double to Quad (FdMULq)
- Ancillary State-Register access instructions (RDASR, WRASR), of which RDY/WRY and STBAR are subcases
- NOP (“promoted” from being a pseudo-instruction)

FQ Optional

The floating-point queue (FQ) is now optional for SPARC implementations that choose to make floating-point traps precise instead of deferred.

New FSR.*ftt* Value

A new value, `invalid_fp_register`, is defined for the FSR.*ftt* field. Use of the new value is optional. If implemented, its use indicates attempted execution of an instruction that refers to an invalid floating-point register number.

What’s New? — the Manual

The SPARC Architecture Manual itself has changed since Version 7.

- Text has been clarified throughout and known errors corrected.
- The index has been considerably expanded.
- A table of synthetic instructions has been added to Appendix A (*Suggested Assembly Language Syntax*).
- Appendix D (*Software Considerations*) and Appendix F (*Opcodes*) have been enhanced.
- Appendixes G through N are completely new.

Acknowledgments

Architecture Definition

The SPARC Version 7 instruction set was defined by a team of individuals at Sun Microsystems that included Anant Agrawal, Fayé Briggs, Will Brown, Robert Garner, David Goldberg, David Hough, Bill Joy, Steve Kleiman, Tom Lyon, Steven Muchnick, Masood Namjoo, David Patterson, Joan Pendleton, Wayne Rosing, K.G. Tan, and Richard Tuck.

The following additional people contributed to Version 8 of the architecture: Michel Cekelov, David Ditzel, Jean-Marc Frailong, Peter Hsu, Eric Jensen, Mike Powell, and Pradeep Sindhu.

Authors

The bulk of the manual was written by Robert Garner of Sun Microsystems. Appendixes were contributed as follows: Appendixes A and G: David Weaver; Appendixes B, C, L, and M: Robert Garner; Appendix D: Richard Tuck and David Weaver; Appendix E: Richard Tuck; Appendix F: Robert Cmelik; Appendix H: Steve Kleiman and David Ditzel; Appendix I: Robert Garner and Ed Kelly; Appendixes J and K: Pradeep Sindhu; and Appendix N: David Hough.

Editors

Robert Garner, Steve Kleiman, Steven Muchnick, and Mike Bechler have served as editors of the SPARC Architecture specification. The editor for the Version 8 specification was David Weaver.

Reviewers

The thoughtful criticisms and suggestions of many colleagues have added much to the readability, completeness, and accuracy of this manual. The editors would like to particularly thank employees at SPARC International member companies, too numerous to list here, for their valuable suggestions and feedback on earlier versions of this document.

Book Production

The production editor for the book edition of this specification was Bobbie Madsen. SPARC-generated computer images on the cover were provided by Sun Microsystems, Inc.

Special Appreciation

Special appreciation is extended to Robert Garner, Bill Joy, Dave Patterson, and Anant Agrawal, who guided and gave form to the definition of SPARC. Robert served as principal architect, and also invested copious amounts of time and energy in the development and enhancement of Versions 0 (9/84) through 7 (10/87) of this document.