
Contents

Chapter 1	Introduction	1
1.1.	SPARC Attributes	1
	Design Goals	1
	Register Windows	1
1.2.	SPARC System Components	2
	Reference MMU	2
	Supervisor Software	2
	Memory Model	2
1.3.	SPARC Compliance Definitions	2
1.4.	SPARC Features	3
1.5.	Conformability to SPARC	4
1.6.	Fonts in Manual	4
1.7.	Notes	5
1.8.	Glossary	5
1.9.	References	7
Chapter 2	Overview	9
2.1.	SPARC Processor	9
	Integer Unit (IU)	9
	Floating-point Unit (FPU)	10
	Coprocessor (CP)	10
2.2.	Instructions	11
	Load/Store	11
	Alignment Restrictions	11

Addressing Conventions	11
Load/Store Alternate	11
Separate I&D Memories	12
Arithmetic/Logical/Shift	12
Control Transfer	12
State Register Access	13
Floating-Point/Coprocessor Operate	13
2.3. Memory Model	13
Input/Output	14
2.4. Traps	14
Trap Categories	14
Chapter 3 Data Formats	17
Chapter 4 Registers	23
4.1. IU <i>r</i> Registers	23
Windowed <i>r</i> Registers	24
Overlapping of Windows	24
Doubleword Operands	25
Special <i>r</i> Registers	25
Register Usage	25
4.2. IU Control/Status Registers	28
Processor State Register (PSR)	28
PSR_implementation (<i>impl</i>)	28
PSR_version (<i>ver</i>)	28
PSR_integer_cond_codes (<i>icc</i>)	28
PSR_negative (<i>n</i>)	28
PSR_zero (<i>z</i>)	29
PSR_overflow (<i>v</i>)	29
PSR_carry (<i>c</i>)	29
PSR_reserved	29
PSR_enable_coprocessor (EC)	29
PSR_enable_floating-point (EF)	29

PSR_proc_interrupt_level (PIL)	29
PSR_supervisor (S)	29
PSR_previous_supervisor (PS)	29
PSR_enable_traps (ET)	29
PSR_current_window_pointer (CWP)	29
Window Invalid Mask Register (WIM)	30
Trap Base Register (TBR)	31
TBR_trap_base_address (TBA)	31
TBR_trap_type (<i>tt</i>)	31
TBR_zero (0)	31
Multiply/Divide Register (Y)	32
Program Counters (PC, nPC)	32
Ancillary State Registers (ASR)	32
IU Deferred-Trap Queue	33
4.3. FPU <i>f</i> Registers	33
Double and Quad Operands	33
4.4. FPU Control/Status Registers	34
Floating-Point State Register (FSR)	34
FSR_rounding_direction (RD)	34
FSR_unused (<i>u</i>)	35
FSR_trap_enable_mask (TEM)	35
FSR_nonstandard_fp (NS)	35
FSR_reserved (<i>res</i>)	35
FSR_version (<i>ver</i>)	35
FSR_floating-point_trap_type (<i>ftt</i>)	35
<i>ftt</i> = IEEE_754_exception	37
<i>ftt</i> = unfinished_FPop	37
<i>ftt</i> = unimplemented_FPop	37
<i>ftt</i> = sequence_error	37
<i>ftt</i> = hardware_error	37
<i>ftt</i> = invalid_fp_register	37
FSR_FQ_not_empty (<i>qne</i>)	38
FSR_fp_condition_codes (<i>fcc</i>)	38

FSR_accrued_exception (<i>aexc</i>)	38
FSR_current_exception (<i>cexc</i>)	38
Floating-Point Exception Fields	39
FSR_invalid (<i>nvc, nva</i>)	39
FSR_overflow (<i>ofc, ofa</i>)	39
FSR_underflow (<i>ufc, ufa</i>)	39
FSR_division-by-zero (<i>dzc, dza</i>)	40
FSR_inexact (<i>nxc, nxa</i>)	40
FSR Conformance	40
Floating-Point Deferred-Trap Queue (FQ)	40
4.5. CP Registers	41
Chapter 5 Instructions	43
5.1. Instruction Execution	43
5.2. Instruction Formats	43
Instruction Fields	44
5.3. Instruction Categories	46
Load/Store Instructions	46
Alignment Restrictions	46
Addressing Conventions	47
Address Space Identifiers (ASIs)	48
Separate Instruction Memory	49
Input/Output	49
Integer Arithmetic Instructions	49
Set Condition Codes	50
Shift Instructions	50
Set High 22 Bits	50
Integer Multiply/Divide	50
Tagged Add/Subtract	50
Control-Transfer Instructions (CTIs)	50
CTI Categories	50
Delay Instruction	51
Delayed Transfer	52

Conditional Delayed Transfer	52
Conditional with $a = 1$	52
Conditional with $a = 0$	53
Unconditional Delayed Transfer	53
CALL and JMPL Instructions	54
SAVE Instruction	54
RESTORE Instruction	54
Trap (Ticc) Instruction	55
Delayed Control-Transfer Couples (DCTI)	55
First-Taken Case	55
First-Untaken Case	55
Read/Write State Registers	56
Floating-Point Operate (FPop) Instructions	56
Coprocessor Operate (CPop) Instructions	57
Chapter 6 Memory Model	59
6.1. Basic Definitions	60
Real Memory	60
Input/Output Locations	60
Overview of Model	61
6.2. Total Store Ordering (TSO)	64
6.3. Partial Store Ordering (PSO)	65
6.4. Mode Control	66
6.5. FLUSH: Synchronizing Instruction Fetches with Memory Operations	66
Chapter 7 Traps	69
7.1. Trap Categories	69
Precise Trap	69
Deferred Trap	70
Interrupting Trap	70
7.2. Trap Models	71
Default Trap Model	71

Enhanced Trap Model	72
7.3. Trap Control	73
ET and PIL Control	73
TEM Control	74
7.4. Trap Identification	74
Trap Type (<i>tt</i>)	74
Error Mode	75
Reset Trap	75
Trap Priorities	75
7.5. Trap Definition	77
7.6. Exception/Interrupt Descriptions	77
Appendix A Suggested Assembly Language Syntax	81
A.1. Notation Used	81
A.2. Syntax Design	84
A.3. Synthetic Instructions	85
Appendix B Instruction Definitions	87
B.1. Load Integer Instructions	90
B.2. Load Floating-point Instructions	92
B.3. Load Coprocessor Instructions	94
B.4. Store Integer Instructions	95
B.5. Store Floating-point Instructions	97
B.6. Store Coprocessor Instructions	99
B.7. Atomic Load-Store Unsigned Byte Instructions	101
B.8. SWAP Register with Memory Instruction	102
B.9. SETHI Instruction	104
B.10. NOP Instruction	105
B.11. Logical Instructions	106
B.12. Shift Instructions	107
B.13. Add Instructions	108
B.14. Tagged Add Instructions	109
B.15. Subtract Instructions	110

B.16. Tagged Subtract Instructions	111
B.17. Multiply Step Instruction	112
B.18. Multiply Instructions	113
B.19. Divide Instructions	115
B.20. SAVE and RESTORE Instructions	117
B.21. Branch on Integer Condition Codes Instructions	119
B.22. Branch on Floating-point Condition Codes Instructions	121
B.23. Branch on Coprocessor Condition Codes Instructions	123
B.24. Call and Link Instruction	125
B.25. Jump and Link Instruction	126
B.26. Return from Trap Instruction	127
B.27. Trap on Integer Condition Codes Instruction	129
B.28. Read State Register Instructions	131
B.29. Write State Register Instructions	133
B.30. STBAR Instruction	136
B.31. Unimplemented Instruction	137
B.32. Flush Instruction Memory	138
B.33. Floating-point Operate (FPop) Instructions	140
Convert Integer to Floating point Instructions	141
Convert Floating point to Integer Instructions	142
Convert Between Floating-point Formats Instructions	143
Floating-point Move Instructions	144
Floating-point Square Root Instructions	145
Floating-point Add and Subtract Instructions	146
Floating-point Multiply and Divide Instructions	147
Floating-point Compare Instructions	148
B.34. Coprocessor Operate Instructions	149
Appendix C ISP Descriptions	151
C.1. ISP Notation	151
C.2. Processor External Interface Definition	152
Interface Macros	153
Interface Signals	153

C.3. Register Field Definitions	154
C.4. Instruction Field Definitions	156
C.5. Processor States and Instruction Dispatch	156
C.6. Instruction Dispatch	159
C.7. Floating-point Execution	160
C.8. Traps	161
C.9. Instruction Definitions	163
Load Instructions	163
Store Instructions	165
Atomic Load-Store Unsigned Byte Instructions	168
Swap Register with Memory Instructions	171
Logical Instructions	172
SETHI Instruction	172
NOP Instruction	172
Shift Instructions	172
Add Instructions	173
Tagged Add Instructions	173
Subtract Instructions	174
Tagged Subtract Instructions	174
Multiply Step Instruction	175
Multiply Instructions	175
Divide Instructions	176
SAVE and RESTORE Instructions	177
Branch on Integer Condition Instructions	178
Floating-Point Branch on Condition Instructions	179
Coprocessor Branch on Condition Instructions	180
CALL Instruction	180
Jump and Link Instruction	180
Return from Trap Instruction	181
Trap on Integer Condition Instructions	182
Read State Register Instructions	182
Write State Register Instructions	183
Store Barrier Instruction	183

Unimplemented Instruction	183
Flush Instruction Memory	184
C.10. Floating-Point Operate Instructions	184
Convert Integer to Floating-Point Instructions	185
Convert Floating-Point to Integer	185
Convert Between Floating-Point Formats Instructions	185
Floating-Point Move Instructions	185
Floating-Point Square Root Instructions	185
Floating-Point Add and Subtract Instructions	186
Floating-Point Multiply and Divide Instructions	186
Floating-Point Compare Instructions	187
Appendix D Software Considerations	189
D.1. Registers	189
<i>In</i> and <i>Out</i> Registers	189
<i>Local</i> Registers	191
Register Windows and %sp	191
<i>Global</i> Registers	192
Floating-Point Registers	192
D.2. The Memory Stack	194
D.3. Functions Returning Aggregate Values	196
D.4. Tagged Arithmetic	197
D.5. Leaf Procedure Optimization	198
D.6. Example Code	200
D.7. Register Allocation Within a Window	201
D.8. Other Register Window Usage Models	202
Appendix E Example Integer Multiplication and Division	
Routines	205
E.1. Signed Multiplication	206
E.2. Unsigned Multiplication	209
E.3. Division	212
Program 1	212

Program 2	213
Program 3	215
Program 4	217
Program 5	219
Program 6	221
Appendix F Opcodes and Condition Codes	227
Appendix G SPARC ABI Software Considerations	233
G.1. SPARC International, Inc.	233
G.2. SCD 1.0 and SCD 2.0	233
G.3. SPARC ABI Software	234
G.4. Register Usage	234
G.5. The Memory Stack	234
G.6. Instruction Set	234
SWAP instruction	235
MUL instructions	236
DIV instructions	236
FSQRTs, FSQRTd instructions	237
FsMULd instruction	237
Quad-precision floating-point instructions	237
Coprocessor instructions	238
Read/Write ASR instructions	239
STBAR instruction	239
G.7. Self-Modifying Code	239
G.8. Non-Standard Floating-Point Operation	239
G.9. Instruction Scheduling	240
Appendix H SPARC Reference MMU Architecture	241
H.1. Introduction	241
H.2. Overview	241
H.3. Software Architecture	242
Contexts	246

Page Table Descriptors	246
Page Table Entry	247
MMU Flush and Probe Model	249
Flush Operations	250
Probe Operations	251
H.4. Hardware Architecture	252
Accessing MMU Registers	252
Control Register	253
Context Table Pointer Register	254
Context Register	254
Diagnostic Registers	255
H.5. Fault Status Register	256
H.6. Fault Address Register	258
H.7. Operation	259
Reset	259
Miss Processing	259
Referenced and Modified Bit Updates	259
Appendix I Suggested ASI Assignments for SPARC Systems	261
I.1. Introduction	261
I.2. ASI Summary	262
I.3. Detailed Descriptions	264
Appendix J Programming with the Memory Model	269
J.1. Memory Operations	269
J.2. Processors and Processes	269
J.3. Portability and Recommended Programming Style	269
J.4. Spin Locks	271
J.5. Producer-Consumer Relationship	272
J.6. Process Switch Sequence	273
J.7. Dekker's Algorithm	274
J.8. Code Patching	275
J.9. Fetch and Add	277

J.10. Barrier Synchronization	279
Appendix K Formal Specification of the Memory Model	281
K.1. Notation	281
K.2. Total Store Ordering	283
K.3. Partial Store Ordering	285
K.4. FLUSH: Synchronizing Instruction Fetches with Memory Operations	287
Appendix L Implementation Characteristics	289
L.1. PSR <i>impl</i> and <i>ver</i> Values	289
L.2. FSR <i>ver</i> Values	290
L.3. Characteristics of Existing Implementations	291
Unimplemented Instructions	292
FLUSH Instruction	292
Integer Deferred-Trap Queue	293
Floating-point Deferred-Trap Queue (FQ) and STDFQ Instruction	293
FSR_nonstandard_fp	293
FPU Exceptions	293
Trap Model and Trap Types	294
Memory Model and STBAR Instruction	294
Ancillary State Registers	294
Width of Load/Store Effective Address	294
Number of Windows	294
Instruction Timing	295
Appendix M Instruction Set Summary	297
Appendix N SPARC IEEE 754 Implementation Recommendations	299
N.1. Misaligned floating-point data registers	299
N.2. Reading an empty FQ	299
N.3. Traps inhibit results	299

N.4. NaN operand and result definitions	300
Untrapped floating-point result in different format from operands	300
Untrapped floating-point result in same format as operands	300
N.5. Trapped Underflow definition (UFM=1)	301
N.6. Untrapped underflow definition (UFM=0)	301
N.7. Integer overflow definition	302
N.8. Nonstandard mode	302
Index	305